CLAIMS

1. A semiconductor device, comprising:

a well of a first conductive type formed in an upper layer of a substrate;

a low-concentration layer of the first conductive type having a lower impurity concentration than the well, the low-concentration layer being formed in an extreme surface layer of a channel portion of the well;

a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, the high-k gate dielectric layer being formed on the low-concentration layer;

a gate electrode formed on the high-k gate dielectric layer; and

source/drain regions of a second conductive type formed in an upper layer of the well, the source/drain regions sandwiching the low-concentration layer.

2. A complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising:

a p-type well formed in an upper layer of a substrate of the n-type circuit region;

a n-type well formed in an upper layer of the substrate of the p-type circuit region;

a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, the p-type low-concentration layer having a lower impurity concentration than the p-type well;

a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, the n-type low-concentration having a lower impurity concentration than the n-type well;

a high-k gate dielectric layer formed on the p-type and n-type low-concentration layers, the high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film;

a gate electrode formed on the high-k gate dielectric layer;

n-type source/drain regions formed in an upper layer of the p-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer; and

p-type source/drain regions formed in an upper layer of the n-type well, the p-type source/drain regions sandwiching the n-type low-concentration layer.

3. A method for manufacturing a semiconductor device, comprising:

forming a well by implanting a first conductive type impurity into a substrate;

implanting a second conductive type impurity into an extreme surface layer of a channel portion of the well;

forming, on the substrate, a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, after implanting the second conductive type impurity;

forming a gate electrode material film to be a gate electrode on the high-k gate dielectric layer;

forming a gate electrode by patterning the gate electrode material film and the high-k gate dielectric layer; and

forming source/drain regions by implanting a second conductive type impurity into the substrate by using the gate electrode as a mask.

4. A method for manufacturing a complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising:

forming a p-type well in an upper layer of a substrate of the n-type circuit region;

forming a n-type well in the upper layer of the substrate of the p-type circuit region;

implanting n-type impurities into an extreme surface layer of a channel portion of the p-type well;

implanting p-type impurities into an extreme surface layer of a channel portion of the n-type well;

forming, on the substrate, a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, after implanting the n-type and p-type impurities;

forming a gate electrode material film to be a gate electrode on the high-k gate dielectric layer;

forming a gate electrode by patterning the gate electrode material film and the high-k gate dielectric layer in the n-type and p-type circuit regions;

forming n-type source/drain regions by implanting the n-type impurity into the p-type well by using the gate electrode as a mask; and

forming p-type source/drain regions in the p-type circuit region by implanting the p-type impurity into then-type well by using the gate electrode as a mask.

5. A method for manufacturing a complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising the steps of:

forming a p-type well by implanting boron ions with a dosage of 1×10^{13} atoms/cm^2 into an upper layer of a substrate in the n-type circuit region;

forming a n-type well by implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm^2 into an upper layer of the substrate in the p-type circuit region;

implanting arsenic or phosphorus ions with a dosage of 5 to 8 $\times 10^{12}$ atoms/cm^2 into an extreme surface layer of a channel portion of the p-type well;

implanting boron ions with a dosage of 3 to 5 × 10^{12} atoms/cm^2 into an extreme surface layer of a channel portion of the n-type well;

forming p-type and n-type low-concentration layers on an extreme surface layer of a channel portion of the p-type and n-type wells by diffusing the arsenic or phosphorus and boron ions implanted into the extreme surface layer by performing a heat treatment;

forming a HfAlOx film on the substrate, after performing the heat treatment;

forming a polycrystalline silicon film to be a gate electrode on the HfAlOx film;

forming a gate electrode on the p-type and n-type low-concentration layers via the HfAlOx film by patterning the polycrystalline silicon film and HfAlOx film;

forming n-type source/drain regions by implanting n-type impurities into the p-type well by using the gate electrode as a mask; and

forming p-type source/drain regions in the p-type circuit region by implanting p-type impurities into the n-type well by using the gate electrode as a mask.